1. With respect to the arguments filed 11/30/2011 concerning Section 112-6:

In the paragraph beginning in the last 11 lines on page, applicant appears to argue that Section 112-6 is only invoked if the claim actually used the "means for..." terminology and, thus, alleges that the "unit configured to..." recitations do not invoke Section 112-6. The examiner notes that this argument is contrary to current Office policy - **SEE: Federal Register/Vol.76, No. 26/Wednesday, February 9, 2011 @ first full paragraph of center column on page 7167.**

2. With respect to the limitations of claims 1, 4-9, and 14-16, the following positions have been taken by the examiner.

A) For the record:

1) The examiner notes that, in addition to the "means for ..." terminology, the following non-exhaustive list of non-structural terms may likewise invoke Section 112-6:

a) "mechanism for ...";

b) "module for ...";

c) "device for ...";

d) "unit for ...";

e) "component for ...";

f) "element for ...";

g) "member for ...";

h) "apparatus for ..."

i) "machine for...";

j) "system for ...";

k) etc,...

It is noted, however, that "circuit for" has been determined to be a "structural term" that does not invoke section 112-6.
[e.g., SEE: Federal Register/Vol.76, No. 26/Wednesday, February 9, 2011 @ first full paragraph of center column on page 7167]

It is further noted that alternative expressions substituted for "for" of a "[*means*] for" recitation (e.g., "adapted to", configured to", etc,...) are insufficient denote

structure and, as such, are insufficient to avoid triggering the presumed interpretation/construction under Section 112-6 presumption.
[e.g., Ex parte Rodriguez, 92 USPQ2d 1395].

2) For a computer-implemented means-plus-function claim limitation that invokes 35 112, sixth paragraph, the corresponding structure is required to be more than simply a general purpose computer or microprocessor.[1] The corresponding structure for a computer-implemented function must include the algorithm as well as the general purpose computer or microprocessor.[2] The written description of the specification must at least disclose the algorithm that transformed the general purpose microprocessor to a special purpose computer programmed to perform the claimed function.[3] Applicant may express the algorithm in any understandable terms including as a mathematical formula, in prose, in a flow chart, or in any manner that provides sufficient structure.[4]

B) With respect to claim 1:

1) The recited ***"reproducing unit configured to ...."*** recited in line 3 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to a BD disc drive as described, for example, in paragraphs 112-114 and 119 of the corresponding PG Pub #2007/0003221. As such, this recited "reproducing unit" has been construed as being limited to such a BD disc drive (and equivalents thereof).

2) The recited ***"determining unit configured to ...."*** recited in lines 4-8 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to the PID filter shown @ 110 of Figure 14 and described, for example, in paragraphs 118 of the corresponding PG Pub #2007/0003221. As

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[1] *See Aristocrat Technologies Inc. v. International Game Technology*, 521 F.3d 1328, 1333, 86 USPQ2d. 1235, 1239-1240 (Fed. Cir. 2008)

[2] *See WMS Gaming, Inc. v. International Game Technology*, 184 F.3d 1339, 51 USPQ2d. 1385 (Fed. Cir. 1999)

[3] *See Aristocrat*, 521 F.3d at 1338, 86 USPQ2d. at 1243.

[4] *See Finisar Corp. v The DIRECTV Group Inc*, 523 F.3d 1323, 1340, 86 USPQ2d. 1385 (Fed. Cir. 1999)

such, this recited "determining unit" has been construed as being limited to such a PID filter (and equivalents thereof).

3) The recited ***"selection means for...."*** recited in lines 13-14 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "means" appears to correspond to the switch shown @ 51 of Figure 8 and @ 223 of Figure 12 which is described, for example, in paragraphs 107 of the corresponding PG Pub #2007/0003221. As such, this recited "selection means" has been construed as being limited to such a switch (and equivalents thereof).

4) The recited ***"first scaling unit for...."*** recited in lines 15-16 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to a respective one of the "down converters" shown @ 222 A and B of Figure 12 and described, for example, in paragraphs 0095 of the corresponding PG Pub #2007/0003221. As such, this recited "selection means" has been construed as being limited to such a down converter (and equivalents thereof).

5) The recited ***"second scaling unit for...."*** recited in lines 17-18 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to a respective one of the "down converters" shown @ 222 A and B of Figure 12 and described, for example, in paragraphs 0095 of the corresponding PG Pub #2007/0003221. As such, this recited "selection means" has been construed as being limited to such a down converter (and equivalents thereof).

6) The recited ***"first blending unit configured to ...."*** recited in lines 23-24 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to the multiplier shown @ 21 of Figure 8 and described, for example, in paragraphs 0059 of the corresponding PG Pub #2007/0003221. As such, this recited "blending unit" has been construed as being limited to such a multiplier (and equivalents thereof).

6) The recited ***"second blending unit configured to ...."*** recited in lines 25-26 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong

analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to the multiplier shown @ 23 of Figure 8 and described, for example, in paragraphs 0059 of the corresponding PG Pub #2007/0003221. As such, this recited "blending unit" has been construed as being limited to such a multiplier (and equivalents thereof).

7) The recited ***"first combining means for ...."*** recited in lines 27-28 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to the adder shown @ 24 of Figure 8 and described, for example, in paragraphs 0059 of the corresponding PG Pub #2007/0003221. As such, this recited "combining means" has been construed as being limited to such a multiplier (and equivalents thereof).

8) The recited ***"third blending unit configured to ...."*** recited in lines 29-30 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to the structure shown @ 25 of Figure 8 and described, for example, in paragraphs 0059 of the corresponding PG Pub #2007/0003221. As such, this recited "blending unit" has been construed as being limited to such circuitry (and equivalents thereof).

9) The recited ***"fourth blending unit configured to ...."*** recited in lines 31-32 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to the multiplier shown @ 28 of Figure 8 and described, for example, in paragraphs 0059 of the corresponding PG Pub #2007/0003221. As such, this recited "blending unit" has been construed as being limited to such a multiplier (and equivalents thereof).

10) The recited ***"second combining means for ...."*** recited in lines 33-34 of claim 1 is construed as being a means plus function limitation that invokes 35 U.S.C. 112, sixth paragraph, given: that the claim limitation meets the 3-prong analysis set forth under section 2181 of the MPEP; and that which is set forth above in part "A" of this paragraph. It is noted that this recited "unit" appears to correspond to the adder shown @ 29 of Figure 8 and described, for example, in paragraphs 0059 of the corresponding PG Pub #2007/0003221. As such, this recited "combining means" has been construed as being limited to such a multiplier (and equivalents thereof).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

I. The showing of Yeh et al:

As shown in Figure 4 and 11, Yeh et al. discloses an image synthesizing system which includes:

1) A first image plane memory (e.g., @ 401 of Figure 4) for storing a flow through background video signal;

2) A second plane memory (e.g., @ 403 of Figure 4) for storing a scaled video signal;

3) A selection means (@ 1131 of Figure 11) for combining the video signals, pixel-by-pixel[5], from the first and second plane memories;

4) A third plane memory (@ 405 of Figure 4) for storing graphics information content;

5) A fourth plane memory (@ 407 of Figure 4) for storing interactive graphics information content;

6) A first blending unit (@ 1141 of Figure 11) which, as illustrated an described, is implemented as an additive α-mixer; and

7) A second blending unit (@ 1151 of Figure 11) which, as illustrated and described, is implemented as an additive α-mixer.

[5] The inherent difference between a selector (non-additive mixer) and a blender (additive mixer).

I. Differences:

Claim 1 differs from the showing of Yeh et al only in that:

1) Yeh et al does not disclose details of the circuitry required to supply the various types of images to the image plane memories (@ 401, 403, 405, 407) of Figure 4 (i.e. does not disclose the circuitry required for scaling the scaled video signal & does not disclose the signals as being provided from a recording medium); and

2) Yeh et al does not disclose details of the structure required to implement the first blender (@ 1141) of Figure 11 (e.g., as comprising multipliers for modifying the opacity of the signals being combined).

IV. The showing of Miyamoto et al, Brett et al, Nakayama, and Hung:

A) As is shown in Figure 11, Miyamoto et al discloses an image synthesizing system similar to that described by Yeh et al. To the point, Miyamoto et al describes a system that includes:

1) A first plane memory (@ 1109);

2) A second plane memory (@ 1110);

3) A selection means (@ 1111, 1104);

4) A scaling/reducing unit (e.g., @ 1102);

5) A third plane memory (@ 1113);

6) A fourth plane memory (@ 1112);

7) A first blending unit (@ 1105; 1106); and

8) A second blending unit (@ 1107 and 1108).

Regardless, Miyamoto et al is relied on for its showing of the signal providing circuitry (e.g., elements 105,1101, 1102, 1103, 109, 110 of Figure 11) required to provide the various signals to the image planes (@ 107 of Figure 11) in such synthesizing system and, in particular, that such circuitry:

1) Was known to have received the signals that were to be displayed from AV stream receiving and decoding circuitry (e.g., via elements 104 and 105 of Figure 1); and

2) Was known to have included scaling/reducing unit (@ 1102 of Figure 11) for producing the scaled video signal.

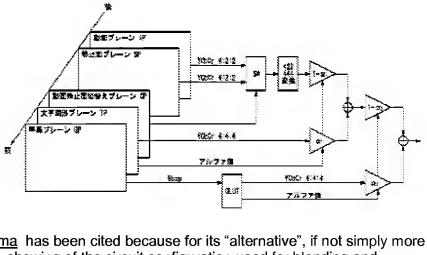
B) The publication titled, "Video Processing For Single Chip DVD Decoder" to Brett et al. is hereby cited to show:

1) Via Figure 5 on page 390, image plane combining circuitry comprised of six image planes, including an additional background image plane, and the required blending circuitry needed to blend the data from the image planes into a composite image [see discussion on page 289 under heading "7. Video Output Processing"]; and

1) Via Figures 5 and 6 on page 390, image plane combining circuitry that located "first" and "second" V/H scaling circuitry within the video processing channel of the video image planes prior to blending [SEE "VSU" of Figure 6]

C) As shown in Figure 1 (reproduced below), Nakayama illustrates conventional image synthesizing circuitry that is analogous to that shown in the applied prior art discussed above; i.e., Yeh et al. and Miyamoto et al.

【図１】



Nakayama has been cited because for its "alternative", if not simply more detailed, showing of the circuit configuration used for blending and combining the data of the character/graphics planes (@ CP, GP) with the

selected data, i.e., selected pixel-by-pixel (@ "SW"), of the respective image planes (@ VP, SP). As illustrated, the blending/combining circuitry includes respective sets of α blending units [i.e., @ α1 & (1- α1) and @ α2 & (1- α2)] for adjusting the opacity of the data being combined/blended followed by respective adding units.

D) Hung is cited, as set forth above in part I of this paragraph, because it evidences that with respect to such synthesis systems, e.g., that described by Miyamoto et al, the AV decoder was known to have received the AV stream from any of various known alternative sources - including a recording media (SEE Figure 3) ; i.e., and more specifically, comprised of a "***reproducing unit***" and a "***determining unit***" as addressed in part I above.

IV. Obviousness:

A) It would have been obvious to one of ordinary skill in the art to have modified the system disclosed by Yeh et al in accordance with the teaching of Miyamoto et al whereby the providing circuitry of Miyamoto et al (e.g., elements 105, 1101, 1102, 1103, 109, 110 in Figure 11) is utilized to decode an AV stream and provide the appropriately decoded/scaled components to the respective plane memories (@ 401, 403, 405, 407 of Figure 4) of the Yeh et al system for synthesis by the synthesizing circuitry of Figure 11. The examiner maintains that Miyamoto et al simply represents the "prior art" on which Yeh et al relied for such details given that that Yeh et al does not specify the circuitry that was required to provide such signals (i.e., the motivation for the modification);

And, while the AV stream in Miyamoto et al was provided via a broadcast, Figure 3 of Hung evidences that a recording medium (@ 308) was a known and obvious alternative source of the AV stream in the modified system.

B) That, in accordance with the teachings of Brett et al.:

1) It would have been obvious to have place the scaling circuitry within the respective image processing channels themselves; i.e., to have provided the scaling using dedicated processing circuitry as opposed to a software driven processor (advantageously reducing required processing power of the display circuitry); and

2) To have "located" an addition background plane at the bottommost level;

C) And while Yeh et al does not disclose the structure required to implement the α-"blenders" of the modified system (e.g., @ 1141 and 1151 of Figure 11 Yeh et al), the examiner contends that the circuit structure required to implement such α-"blenders" was notoriously well known in the video mixing arts as evidenced via Figure 1 of Nakayama in the "same" environment. As such, the examiner maintains that it would been obvious to have implemented the blenders in the modified system of Yeh et al using the conventional configuration shown in Figure 1 of Nakayama given that the Nakayama at least represents an "alternative" configuration of said circuitry; e.g., it was obvious to substitute one embodiment for the other.

****

Concerning the amendments and arguments of 11/30/2011:

1) Figure 3 of Hung, labeled "GENERAL PLAYBACK DIAGRAM", is maintained to be indicative of notoriously well known reproduction apparatus circuitry used in the reproduction and display of a conventional MPEG-2 transport stream. This showing evidences that it was well known for such conventional playback apparatus to have comprised:

1) A storage media reproduction device (e.g., @ 308) comprised of an optical disc drive unit for reproducing an MPEG-2 transport stream content for an optical disc **[e.g., see lines 20-21 of column 7] -** i.e., wherein this structure corresponds to the recited "***reproducing unit configured to…***" set forth in line 4 of claim 1; and

2) An MPEG-2 element stream demultiplexer (e.g., @ 312) which receives the reproduced MPEG-2 transport stream content from the reproducing unit (@ 308) and separates theMPEG-2 transport stream content into respective MPEG-2 elemental streams which are provided to respective decoding and display channels **[e.g., see lines 20-40 column 7] -** i.e., wherein such an MPEG-2 transport stream demultiplexer is implicitly controlled by and MPEG-2 PID filter as required to detect and separate the respective TDM multiplexed elemental streams (for control of the timing of the demultiplexing process). Such implicit PID filtering circuitry corresponds to the recited "***determining unit configured to…***" set forth in line 5-9 of claim 1.

2) The examiner notes that the positional arrangement of the plane memories now recited in the last four lines of claim 1 does not appear to be a structural limitation, rather it appears to refer to the apparent depth of the planes the which is a function of the blending circuitry/operation. The examiner maintains that the applied prior art renders obvious the

recited blending circuitry arrangement of claim 1 for reasons set forth above and, as such, implicitly evidences the apparent depth of the plane now recited in the last four line of claim 1.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 1.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 4, further in view of US Patent #6,661,426 to Jetha et al. Additionally:

1) It is noted that, in Figure 4, Yeh et al indicates that the background video plane (@ 401) can contain video representing a "Fixed Pattern". The examiner maintains that such a video is, by definition, a "wallpaper picture".

2) Alternatively, Jetha et al has been cited because it evidences that it was known, in the video image compositing arts, to have provided and utilized "wallpaper picture data" as a background image for the combined image signals [e.g., note lines 10-14 of column 4]. In light this showing, it would have been obvious to one of ordinary skill in the art to have provided such a wallpaper

picture signal to the background plane (@ 401 in Figure 4 of Yeh et al) in the modified system of Yeh et al.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 1. Additionally:

A) The examiner maintains that it was well known, and would have been obvious, for one of the graphics planes in the modified system of Yeh et al to have comprised or included subtitle information (e.g., Note: lines 32-35 of Miyamoto et al; and elements 316 and 318 in Figure 3 of Hung); and

B) The examiner maintains that the mixing ratios are necessarily "based on" the data that is mixed in at least the mixing ratio is necessarily set to mix the signals according to image position and/or image priority .

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 6.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 1. Additionally:

Claim 9 further differs from the modified system of Yeh et al in that claim 9 requires an additional frame/plane memory to be located at the output of the selection means.

The examiner takes Official Notice that it was well known in the video compositing art to have associated an additional frame/plane memory with the display device to compensate for differences in the refresh rate of the sources and the display rate of the display device. In light this conventional knowledge, it would have been obvious to one of ordinary skill in the art to have associated such a frame/plane memory with the display in the modified systems of Yeh et al. to compensate for differences in display and refresh rates.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 1. Additionally:

The examiner maintains that the mixing ratios are necessarily "based on" the data that is mixed in at least the mixing ratio is necessarily set to mix the signals according to image position and/or image priority

The examiner notes that the priority information determines "transparency". Thus, any time/position at which one images (e.g., the reduced images) are displayed over/through another image inherently requires the non-displayed image to be transparent at that location.

11. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 4, further in view of US Patent #6,661,426 to Jetha et al. Additionally:

It is noted that, in Figure 4, Yeh et al indicates that the background video plane (@ 401) can contain video representing a "Fixed Pattern". The examiner maintains that such a video is, by definition, a "wallpaper picture".

Jetha et al has been cited because it evidences that it was known, in the video image compositing arts, to have provided and utilized "wallpaper picture data" as a background image for the combined image signals [e.g., note lines 10-14 of column 4]. In light this showing, it would have been obvious to one of ordinary skill in the art to have provided a wallpaper picture signal to one of the frame stores in the modified system of Yeh et al as background image data for the combined image; i.e., again the examiner notes that the priority information determines "transparency" and, as such, any time/position at which one images (e.g., the wallpaper image) is displayed over/through another image such inherently requires the non-displayed image to be transparent at that position/location. When the wallpaper image it not displayed over/through another image, it is display at "other" areas,

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 1.

13. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent #7,623,140 to Yeh et al. in view of:

A) US Patent #7,496,278 to Miyamoto et al;

B) The article titled, "Video Processing For Single-Chip" DVB Decoder" by Brett et al.

C) US Patent #7,676,142 to Hung;

D) Japanese Patent Document #2003-259213 to Nakayama.

for the same reasons that were set forth above with respect to claim 1, in further in view of the 1984 publication "Structured Computer Organization" by Tanenbaum.

Tanenbaum has been cited as evidencing the fact that those of ordinary skill in the art have long recognized hardware and software implementations of a given processing operation to be obvious and equivalent [note lines 10-13 of page 11]. In light of this showing, the examiner maintains that it would have been obvious to one of ordinary skill in the art to have implanted the modified system of Yeh et al. using a software driven processor (i.e., wherein the software must necessary be stored via some type of processor readable medium).

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID E. HARVEY whose telephone number is (571) 272-7345. The examiner can normally be reached on M-F from 6:00AM to 3PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. William Vaughn, can be reached on (571) 272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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